IN THE CLAIMS:

1. - 13. (Canceled)

14. (Original) A method of forming a semiconductor device comprising:

(a) forming isolation layers in predetermined regions of a semiconductor substrate to define a first region, a second region and a third region;

(b) forming a first gate insulating layer and a first gate conductive pattern stacked sequentially on the first region, a second gate insulating layer and a second gate conductive pattern stacked sequentially on the second region, and a third gate insulating layer and the second gate conductive pattern stacked sequentially on the third region; and

(c) patterning together the first gate conductive pattern and the second gate conductive pattern to form a first gate electrode, a second gate electrode and a third gate electrode in the first, second and third regions, respectively,

wherein the first gate insulating layer, the second gate insulating layer and the third insulating layer are formed having varying thicknesses and each layer has a different thickness than the other layers.

15. (Original) The method of claim 14, wherein the (b) step comprises:

forming the first gate insulating layer and the first gate conductive pattern stacked sequentially on the first region;

forming a second gate conductive layer on the entire surface of the semiconductor substrate having the second and third gate insulating layers; and

patterning the second gate conductive layer to form the second gate conductive pattern exposing the first gate conductive pattern in the first region.

16. (Original) The method of claim 15, wherein forming the first gate insulating layer and the first gate conductive pattern comprises:

forming the first gate insulating layer on the first region;

forming a first gate conductive layer on the semiconductor substrate having the first gate

insulating layer; and

patterning the first gate conductive layer to form the first gate conductive pattern and a capacitor lower electrode, the first gate conductive pattern is disposed in the first region and the capacitor lower electrode is disposed on a predetermined region of the isolation layers.

17. (Original) The method of claim 16, after patterning the first gate conductive layer, further comprising:

forming a dielectric layer on the semiconductor substrate having the first gate conductive pattern and the capacitor lower electrode;

patterning the dielectric layer to form a dielectric pattern, the dielectric pattern exposes the second and third regions and covers the first conductive pattern and the capacitor lower electrode.

18. (Original) The method of claim 17, wherein the dielectric layer is a material selected from the group consisting of silicon oxide, silicon nitride, oxide-nitride-oxide, tantalum oxide, barium-strontium-titanium oxide, zirconium oxide, hafnium oxide, plumbum-zinc-titanium oxide, strontium-bismuth-tantalum oxide, and any combination thereof.

19. (Original) The method of claim 17, further comprising forming an anti-reflecting layer on the second gate conductive layer, before patterning the second gate conductive layer,

wherein forming the anti-reflecting layer comprises selecting a material and controlling a thickness of the selected material for the anti-reflecting layer to provide, in the step (c), the anti-reflecting layer having a non-selective etching characteristic with respect to the dielectric layer.

20. (Original) The method of claim 17, wherein forming the second gate conductive pattern comprises forming a capacitor upper electrode on the dielectric pattern opposite the capacitor lower electrode.

21. (Original) The method of claim 17, wherein the step (c) further comprises forming a capacitor upper electrode on the dielectric pattern opposite the capacitor lower electrode.

22. (Original) The method of claim 14, wherein the first gate conductive pattern and the second conductive pattern are formed of the same material.

23. (Original) The method of claim 22, wherein the first gate conductive pattern and the second conductive pattern are formed of polycrystalline silicon.

24. (Original) The method of claim 14, wherein the first gate insulating layer is silicon dioxide with a thickness of between about 50 Å to about 300 Å formed by thermal oxidation;

the second gate insulating layer is silicon dioxide with a thickness of between about 10 Å to about 100 Å formed by thermal oxidation; and

the third gate insulating layer is silicon dioxide with a thickness of between about 100 Å to about 1000 Å formed by a chemical vapor deposition.